Improved Contact Formation for Large Area Solar Cells Using the Alternative Seed Layer (ASL) Process

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Abstract – **Light induced plating (LIP) chemistry and tooling that are scalable to industrial solar cell processing are used to deposit layers of nickel (Ni), copper (Cu), and tin (Sn) on previously defined front grid patterns of large area solar cells. The Ni plated layer is in direct contact with the silicon surface enabling the formation of a nickel silicide (NiSi) contact after annealing. This Alternative Seed Layer (ASL) process involves many variables that influence the formation of the NiSi contact. This paper will investigate two different aspects of the contact formation: 1) the position of the annealing step in the process flow; i.e. after Ni plating or after Ni/Cu plating and 2) the resulting contact formation for monocrystalline silicon (mono-Si) versus polycrystalline silicon (poly-Si) substrates. A decrease in the series resistance (R_{series}) measurement and increase in efficiency after annealing has been demonstrated for both mono-Si and poly-Si cells with Ni only and Ni/Cu annealing.**

Index Terms – **annealing, copper, contact, electrochemical processes, metallization, nickel, silicon**

I. Introduction

The alternative seed layer (ASL) process coupled with light induced plating (LIP) of nickel (Ni) and copper (Cu) to produce high quality, low cost front metal contacts for industrial high efficiency silicon solar cells has been presented previously [1, 2]. Nickel mono-silicide (NiSi) has been discussed as the favored metal silicide for formation of ohmic contacts in silicon solar cells due to a low silicide formation temperature and low silicon consumption [3]. In addition, nickel can be selectively plated to form self-aligned contacts and has been shown to be an effective barrier to copper diffusion [4]. However, in order to form this NiSi ohmic contact on a silicon solar cell, the ARC layer, typically silicon nitride (SiN_x), must be removed in order to expose a clean silicon surface for nickel plating.

Two of the more common approaches used for patterning the ARC layer are 1) masking & wet chemical etching and 2) laser ablation [5]. Once the ARC layer is removed, the NiSi ohmic contact can be formed by depositing a nickel seed layer directly on the exposed silicon surface and annealing to form NiSi. For solar cells with shallow junction emitters, the NiSi formed must be thin and uniform or the shallow emitter may be shunted [5]. There are multiple processing variables involved in order to achieve a uniform, thin NiSi ohmic contact. This paper will only be investigating the impact of the annealing process on the NiSi contact formation for cells with and without copper metallization. Both monocrystalline silicon (mono-Si) and polycrystalline silicon (poly-Si) large area substrates will be evaluated. Future work to optimize both the incoming cells and the ASL process will be necessary in order to achieve improved electrical performance.

II. Experimental Details

Industrially supplied 125 x 125 mm mono-Si and 156 x 156 mm poly-Si textured solar cells with an n-type emitter, SiN_x ARC layer, and screen printed Al backside are used for these experiments. The cells are laser ablated in order to define the front grid pattern in the ARC layer. The laser ablation process is performed at various facilities resulting in cells with grid lines ranging from 10 to 60 μm wide. The cells tested have emitter sheet resistance's ranging from 60 to 120 Ω/sq.

Figure 1 illustrates the two process sequences used to fabricate these cells, Process A & B. Both process sequences start with incoming cells received with the Al paste backside and the front side ARC deposition. Laser ablation is performed to define the grid pattern in the ARC layer. The ASL process begins with an activation step prior to LIP Ni. Process A continues with an anneal after LIP Ni; whereas, Process B continues with LIP Cu over the LIP Ni followed by an anneal step. As shown in Figure 1 below, Process A has an additional two steps versus Process B.

All the highlighted processing steps in Figure 1 are performed on large area cells using Technic Inc. chemistry and processing equipment. A proprietary activating solution is used to clean the laser ablated solar cells prior to LIP Ni [2]. The nickel, copper, and tin layers are deposited using Technic's LIP plating tool designed to keep the backside of large area solar cells dry during plating. A proprietary nickel solution is used to deposit the nickel seed layer directly on the silicon surface [2]. The copper layer is deposited using TechniSol Cu 2440 [6] and the tin layer is deposited using a proprietary chemistry formulated specifically for LIP. Annealing work is performed using a laboratory scale annealing tool and an industrially scalable annealing tool by Despatch Industries.

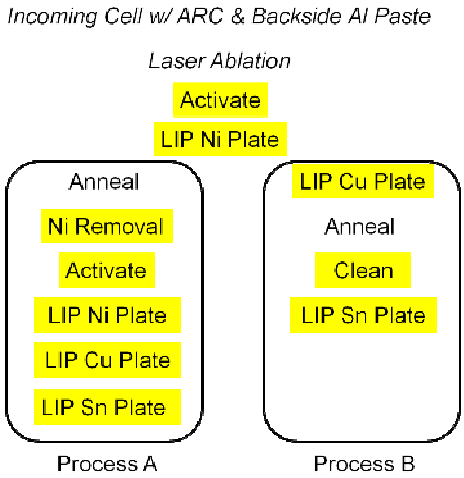

Fig. 1: Alternative Seed Layer (ASL) process. Process A = Anneal after Ni only, Process B = Anneal after Ni/Cu.

The plated grid lines are characterized using scanning electron microscopy (SEM) and x-ray fluorescence (XRF). In addition, the electrical properties of the large area solar cells are measured before and after annealing using a standard flash tester.

III. Results

As shown in Figure 1, prior to the ASL process, the SiN_x ARC layer is patterned using laser ablation. The quality of the laser ablation process can vary from vendor to vendor; therefore, an activating solution has been developed in order to prepare the laser ablated cells for nickel deposition [2]. However, if the laser ablation process does not completely remove the ARC layer in the bus bar and grid line areas, the quality of the nickel plating can be compromised. Figure 2 shows lines patterned using two different laser conditions on one solar cell. The resulting nickel morphology is very different even though the lines were plated at the same time on the same cell.

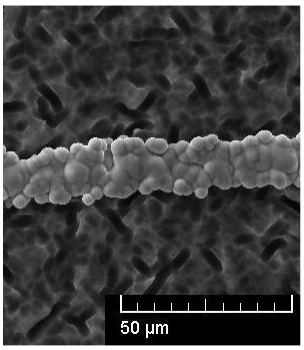

Fig. 2a): Ni morphology from laser process #1.

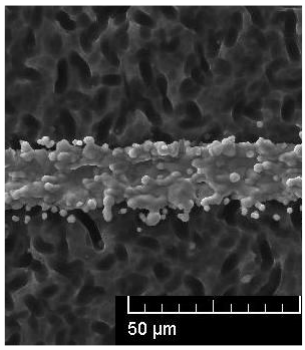

Fig. 2b): Ni morphology from laser process #2.

In addition to the laser ablation process, the nickel plating bath chemistry influences the quality of the nickel deposited on the silicon surface. Figure 3 shows a top down SEM image of a nickel plated grid line. The improved nickel deposit shown in Figure 3b is a result of an optimized plating bath chemistry.

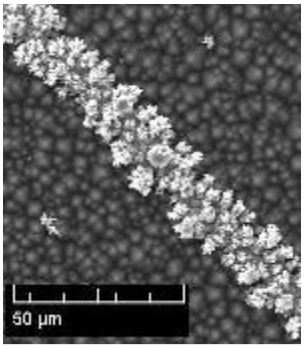

Fig. 3a): Poor Ni deposit due to non-optimized bath

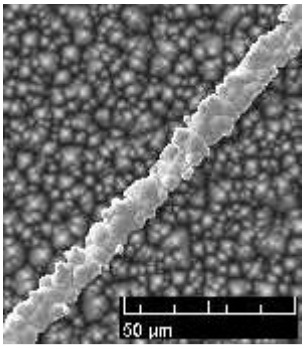

Fig. 3b): Good Ni deposit after bath optimization

The cells plated in this study were laser ablated at various facilities and the laser ablation quality is not always optimized for the ASL process. Therefore, the electrical and mechanical properties of the ASL plated solar cells may be negatively impacted by the laser ablation process. All cells were plated with an optimized Ni plating bath as discussed with Figure 3.

Figure 1 illustrates two different annealing approaches for formation of the NiSi layer. The annealing takes place after LIP Ni for Process A and after LIP Ni/Cu for Process B. The advantages and disadvantages of both processes are listed in Table 1.

Table 1: Advantages and Disadvantages of Annealing after Ni (Process A) versus after Ni/Cu (Process B)

Advantages	Disadvantages	
• Thin deposited Ni layer prior to anneal • No Cu diffusion during anneal	• Annealing atmosphere more critical • Possible adhesion issue between Si & 2nd Ni layer • More process steps	Anneal after Ni
• Good adhesion between Si & Ni • Annealing atmosphere less critical • Less process steps	• Risk of Cu diffusion into Si • Thick Ni deposit required as Cu barrier prior to anneal	Anneal after Cu

Proof of concept experiments to determine the electrical functionality of solar cells processed using Process A and Process B will be discussed. Further investigation will be required to understand the mechanical performance of the different annealing sequences.

A. Mono-Si Process A - Nickel Only Anneal

125 x 125 mm laser ablated mono-Si cells with approximately 10 µm grid lines were processed through

Process A. The emitter sheet resistance is assumed to be ~60 Ω/sq. The annealing condition used will be referred to as High T. After annealing, the residual nickel metal was removed and fresh nickel and copper layers were plated using Technic's LIP plating tools and chemistries. Table 2 shows the electrical results of the annealed cells compared to control cells that have not been annealed.

Table 2: "High T" Anneal: Ni only Mono-Si Cells IV Results

	Voc (mV)	Jsc (mA/cm^2)	%FF	%Eff	R_{series} (Ω·cm^2)
Proc. A	624	35.7	78.9	17.8	0.54
Proc. A	622	35.9	78.5	17.4	0.34
Control	627 (±3)	36.9 (±0.6)	61.7 (±4.1)	14.3 (±1.1)	3.8 (±0.7)

The last column in Table 2 shows the measured series resistance (R_{series}) normalized by cell area. The R_{series} decreases by more than 80% for the annealed cells compared to the non-annealed controls indicating the formation of a good NiSi contact. As a result, the efficiency improves by 3.3 ± 1.1 % and the fill factor increases by 16 ± 4.1%. Therefore, the proof of concept experiments for Process A (Ni only anneal) at "High T" show decent electrical results on mono-Si cells with a 60 Ω/sq emitter layer.

B. Mono-Si Process B – Ni/Cu Anneal

125 x 125 mm cells similar to those used above were processed through Process B. Figure 4 compares the electrical results for Process A (solid line) and Process B (dashed lines) at two annealing conditions. The Jsc is lower for Process A compared to Process B. Process A includes extra processing steps that can cause damage to the SiN_x layer. The damaged areas are more susceptible to extraneous plating which can cause shadowing on the solar cell. This shadowing may reduce the current generated by the solar cell. This type of damage can be avoided in the future by optimizing the additional processing steps to cause less damage to the nitride and by modifying the incoming SiN_x layer.

However, it is still obvious from the IV curves in Figure 4 that the Ni/Cu anneal at High T has significant shunting; whereas, the Ni only anneal cell does not. Therefore, the presence of copper during the High T anneal is detrimental to the electrical performance of the solar cells. The best electrical properties on the mono-Si cells were obtained using a lower thermal budget anneal, Mid T, with Process B. As observed in Figure 4, the IV results from the Mid T anneal do not demonstrate any obvious shunting and the curve is fairly square indicating a good fill factor. Therefore, it appears that the nickel barrier layer is good enough to prevent copper diffusion at the Mid T annealing condition but not at the High T condition.

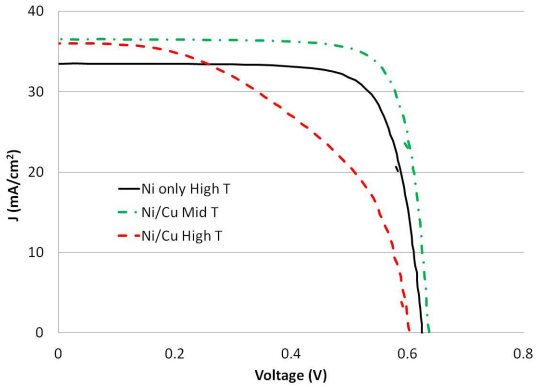

Fig. 4: IV curves of mono-Si cells post anneal

Table 3 lists the IV results for the cells shown in Figure 4. Process B with the Mid T annealing condition has the best results with a fill factor of 79.2% and an efficiency of 18.4%. Therefore, by lowering the thermal budget, it is possible to achieve decent electrical results for the Ni/Cu stack anneal (Process B). Future work will investigate the performance of Process A using a lower thermal budget anneal.

Table 3: IV Results for Ni/Cu vs. Ni only Anneal

	Voc (mV)	Jsc (mA/cm^2)	%FF	%Eff	R_{series} (Ω·cm^2)
Ni only High T	624	33.5	76.8	16.1	0.83
Ni/Cu Mid T	637	36.5	79.2	18.4	0.5
Ni/Cu High T	605	36.4	48.3	10.6	0.34

C. Poly-Si – Process A vs. Process B

Similar testing was performed on 156 x 156 mm poly-Si cells with emitter sheet resistance's ranging from 65 to 120 Ω/sq. Comparison of Process A (Ni only) and Process B (Ni/Cu) at High T for poly-Si cells with a 65 Ω/sq emitter sheet resistance is shown in Figure 5. The Ni only anneal (solid line) demonstrates better results on the poly-Si cells at the High T anneal condition. Significant shunting occurs on the poly-Si cells after annealing the Ni/Cu stacks at High T.

Further testing on 156 x 156 mm poly-Si cells with an emitter sheet resistance of 120 Ω/sq was performed to investigate lower thermal budget anneals. 6 cells total were processed through Process B. 3 cells were annealed at a Mid T condition and 3 cells were annealed at a Low T condition. IV measurements were performed pre and post annealing. Figure 6 compares the R_{series} results pre and post annealing for both groups. The R_{series} decreases by more than 70% after annealing and the variation across samples is reduced.

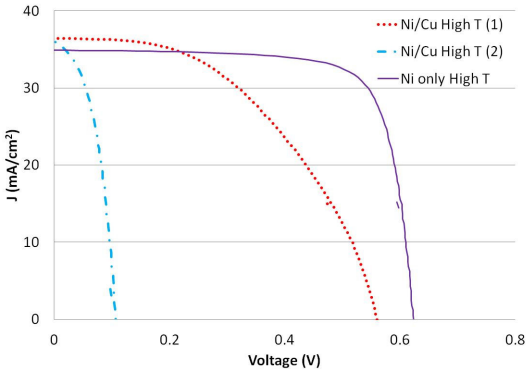

Fig. 5: Comparison of IV results for poly-Si process A (Ni) vs. process B (Ni/Cu) anneal at High T

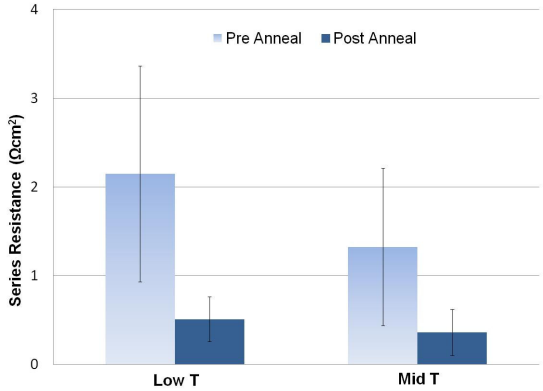

Fig. 6: Pre & Post R_{series} measurements on poly-Si cells

Table 4 compares the post annealing IV results for the Mid T and Low T annealing conditions. There is not a significant difference in the electrical performance of the two annealing conditions.

Table 4: Process B - Poly-Si Mid T & Low T IV Results

	Voc	Jsc (mA/cm^2)	%FF	%Eff	R_{series} ($\Omega \cdot cm^2$)
Low T	617 (± 3)	34.7 (± 0.1)	75.9 (± 1.1)	15.9 (± 0.3)	0.8 (± 0.4)
Mid T	617 (± 2)	34.6 (± 0.2)	76.8 (± 0.9)	16.1 (± 0.2)	0.6 (± 0.4)
Best	620	34.8	77	16.4	0.7

Figure 7 compares the efficiency data collected for both groups before and after annealing. The size of the circles in the graph is a function of the variation within the data. The pre annealing data has ~10x the variation of the post annealing data. The post annealing efficiency for all the cells is very consistent at 16.1 ± 0.2 %, regardless of the pre efficiency measurements. Therefore, it is possible with Process B to achieve repeatable efficiency data on poly-Si cells with a 120 Ω/sq emitter. Little evidence of shunting is observed in the IV curves; however, further testing will be required to ensure the long term stability of cells fabricated using Process B. The best cell performance resulted in an efficiency of 16.4% and a fill factor of 77%.

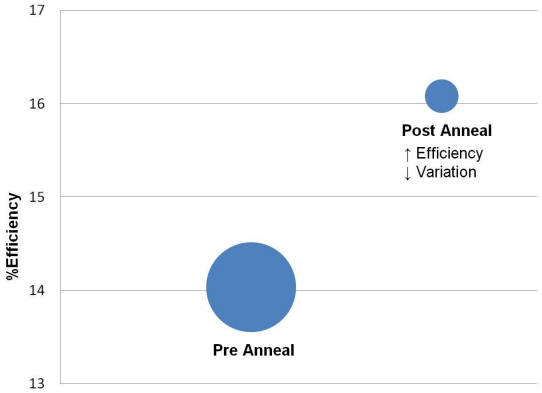

Fig.7: Comparison of %efficiency before and after annealing for poly-Si cells with 120 Ω/sq emitter

IV. Conclusions & Future Work

Preliminary results indicate that a good NiSi contact can be formed using Process A and Process B on mono-Si and poly-Si cells with laser ablated front grid patterning. A large decrease in R_{series} is observed between the non-annealed controls and the annealed samples. A reduced thermal budget that still enables formation of the low resistance NiSi contact is critical to obtain decent electrical results for Process B – annealing with the Ni/Cu stack. With the selection of the appropriate thermal budget, an improvement in efficiency and fill factor for both mono-Si and poly-Si cells is observed.

In addition, poly-Si cells with a high emitter sheet resistance of 120 Ω/sq were successfully processed through the ASL flow using Process B. These cells resulted in very repeatable efficiency numbers at two different annealing conditions. Therefore, the formation of a good NiSi contact with the 120 Ω/sq emitter layer is possible and repeatable.

One of the main disadvantages listed for Process B in Table 1 is the risk of Cu diffusion into the silicon. This study demonstrates that by reducing the thermal budget of the anneal and ensuring a thick enough nickel diffusion barrier, an increase in efficiency can be obtained without obvious shunting per the electrical results. Further studies are required to understand if there are localized shunting problems and to determine the lifetime.

As discussed in Figure 2, the quality of the laser ablated surface can have a significant impact on the morphology of the nickel film deposited. If residual SiN_x is remaining in the grid lines, this will cause an area of the silicon that cannot plate and in essence will result in a porous nickel barrier. Therefore, cells with laser ablation parameters optimized for

the ASL process may significantly improve results obtained by Process A and Process B.

Another important parameter that is not addressed in this study but will be in future work is the adhesion of the metal lines to the silicon. Again, there is a correlation between the laser ablation quality and adhesion of the metal lines. Further work is required to understand the impact of patterning, plating, and annealing on the adhesion of the metal lines.

ACKNOWLEDGEMENTS

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